# Challenges and Chances of Multi Core Processors within Future Control- and Monitoring FADEC

**Karel Stastny**
München
GERMANY

karel.stastny@aes.de

**Keywords**: AVT-357, AES, Multi Core Processors, RTCA DO-178/ C DAL-A; FADEC

## *ABSTRACT*

*A Future military aircraft will request a dramatic increase in calculation capacity to cope with increased expectations regarding information security, ability of big data management, increased control availability and on-board diagnostics and prognostics. To satisfy this expectations and to be prepared for distributed control architectures it is mandatory that within safety critical equipment, high performance multi-core processors are integrated that are compliant to certification constraints.*

*Since AES is developing military FADEC (Full Authority Digital Engine Control), research and technologies for the next generation of FADEC is a key driver. The presentation "Challenges and Chances of multi-core processors within FADEC" shows what the today functionality of a FADEC is and develops the vision of next generation electrical systems within a gas turbine engine (distributed control). Derived from the overall architecture of a future distributed propulsion controls system the key technologies for the future FADEC will be presented.*

*Besides different technologies one major element is the introduction of a certifiable multi-core processor / microcontroller platform for next generation FADEC.*

*Since development cycles of processors are accelerating and multi-core processors are replacing single-core processors it is mandatory to understand the new technology and to identify principles that are mandatory for safety-critical applications.*

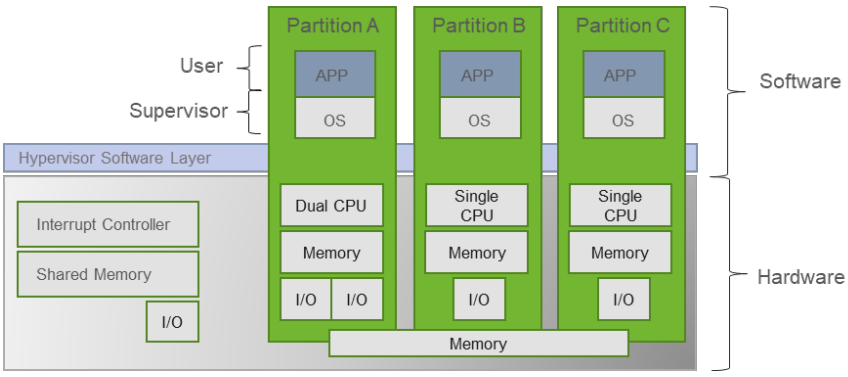


**Figure 1: Principle Micro Controller Processor Architecture for Usage in next generation FADEC**

*This presentation describes the essential characteristics and features of such multicore processors and their architectures that are relevant for a certifiable FADEC. Besides the technical aspects also the today's certification baseline is analysed. Derived from technical and certification investigation an applicable multi-*

*core processor / micro controller concept is presented and assessed regarding the functional safety objectives and existing limitations of modern multi core processors / micro controllers. Finally an implementation road map is discussed that seems to be indispensable to guarantee the safe introduction of multi core processor / micro controller technology into safety critical equipment.*